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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,582	01/12/2006	Celine Juliette Detecheverry	NL03 0878 US1	3317
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NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER BAISA, JOSE LITO SASIS	
			ART UNIT 2832	PAPER NUMBER
			NOTIFICATION DATE 05/27/2008	DELIVERY MODE ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

**Office Action Summary****Application No.**

10/564,582

**Applicant(s)**

DETECHEVERRY ET AL.

**Examiner**

JOSELITO BAISA

**Art Unit**

2832

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 January 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiromoto [JP2001230375A].

Hiromoto discloses a substrate 1 having a first major surface, an inductive element 14b fabricated on the first major surface of the substrate 1, the inductive element 14b comprising at least one conductive line, a plurality of tilling structures (8b, 5b) in at least one layer, wherein the plurality of tilling structures (8b, 5b) are electrically connected together and arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element [Abstract, Paragraphs 12, 13 and 14 Figure 1a and 3].

With respect to limitation, "*plurality of tilling structures arranged to improve manufacturability of semiconductor device*", this has been considered but not given any patentable weight. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the

prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ964, 966 (Fed. Cir. 1985).

With respect to claim 22, the claim is a method counterpart of structure of claim 1 and method steps therefore are inherent for manufacturing a semiconductor device that has tilling structure.

Regarding claim 2, Hiromoto discloses the tilling structures (8b, 5b) being made from tilling structure material, wherein the plurality of tilling structures (8b, 5b) are arranged in a pattern so that the amount of tilling structure material in an area closer to the inductive element is smaller than the amount of tilling structure material in an area farther away from the inductive element [Abstract, see Figure 3].

Regarding claim 3, Hiromoto discloses the tilling structures (8b, 5b) are located at different layers, tilling structures at each layer being arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures (8b, 5b) by a current in the inductive element 14b [Abstract, Paragraph 12, Figure 3].

With respect to limitation, "*wherein the arrangement of the tilling structures is determined by a desired pattern density of the semiconductor device for improving at least one of a process window of lithography, uniformity of Chemical Mechanical Polishing removal rate and integrity of low-k dielectrics*", this has been considered but not given any patentable weight. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does

not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ964, 966 (Fed. Cir. 1985).

Regarding claim 4, Hiromoto discloses the geometrical pattern of tiling structures (8b, 5b) at two different layers is different in shape [Abstract, Figures 1a, 1b and 3].

Regarding claim 5, Hiromoto discloses the tiling structures (8b, 5b) at different layers are electrically connected to each other [Abstract, Paragraph 12, Figures 1b and 3].

Regarding claim 6, Hiromoto discloses the tiling structures (8b, 5b) are connected to a DC potential [Abstract, Figure 3].

Regarding claim 7, Hiromoto discloses the tiling structures (8b, 5b) are a plurality of slender elongate elements [Abstract, Figure 3].

Regarding claim 8, Hiromoto discloses in the tiling structures are a plurality of substantially triangular elements [see Figures 3 or 4].

Applicant has disclosed in Page 12, Lines 19-21, that the tiling structures can be any other suitable shape as long as it improves the Q-factor of the inductive element.

Regarding claim 9, Hiromoto discloses the tilling structures (8b, 5b) are locally oriented perpendicular to the at least one conductive line of the inductive element [Abstract, Figure 1b].

Regarding claim 10, Hiromoto discloses the elements 6 of the tilling structures 8b, 5b are locally oriented perpendicular to the at least one conductive line of the inductive element [Abstract, Figure 2c].

Regarding claim 11, Hiromoto discloses a ground shield 8d for shielding the inductive element 14b from a further layer [Abstract, Figure 1b].

Regarding claim 12, Hiromoto discloses the further layer is the substrate 1 [Abstract, Figure 1b].

Regarding claim 13, connection means electrically connecting the plurality of tilling structures (8b, 5b) with the ground shield 8d without creating a conductive loop [Abstract, Paragraphs 12 and 13, Figures 1b and 3].

Regarding claim 14, Hiromoto discloses the tilling structures (8b, 5b) are formed in a region other than a region directly below the inductive element 14b [Abstract, Figure 1b].

Regarding claim 15, Hiromoto discloses a passive element [Abstract, Figure 3].

Regarding claim 16, Hiromoto discloses the further passive element is a capacitive element [Paragraph 36, Figure 3].

Regarding claim 17, Hiromoto discloses the capacitive element comprises two capacitor electrodes 14b and (8b, 5b) or 8d at least one of the capacitor electrodes being formed by a plurality of tilling structures [Abstract, Figure 3].

Regarding claim 18, Hiromoto discloses a capacitor electrode formed by a plurality of tilling structures (8b, 5b) leads to a metal or polysilicon region density in the inductor vicinity respecting the design rules of advanced IC technologies [ Paragraph 36, Figure 1b].

Regarding claim 19, Hiromoto discloses one capacitor electrode of the capacitive element is formed by the ground shield 8d [Paragraph 36, Figure 1b].

Regarding claim 20, Hiromoto discloses the integration of the capacitive element with the inductive element 14b is optimized to respect the metal pattern density in advanced silicon technologies [Paragraph 36, Figure 1b].

Regarding claim 21, Hiromoto discloses the distance between the capacitive element and the inductive element 14b is large enough to avoid a dominant fringe coupling between them [Paragraphs 12, 13 and 36, Figure 1b].

***Response to Arguments***

Applicant's arguments with respect to claims 1-22 have been considered but are not persuasive.

Applicant argues that the cited portion of Hiromoto appears to be a ground shield instead of a tilling structure. That is not correct.

Hiromoto discloses a layer of polysilicon pattern 5b in between the inductive element 14b and the substrate 1. Metal silicide 8b disposed on polysilicon 5b for the purpose of eliminating the noise generated by coupling of inductive element and the substrate 1. But since eddy current occurs in metal silicide layer lowers down the quality factor Q, Hiromoto introduces slits 15 to eliminate this problem. The slits created a finger-like structure electrically connected to a central strip. Similar to the specified structure of the applicant on Page 8, Lines 10-13. This structure pattern (8b, 5b), tilling structure, has a shape that substantially inhibits an inducement of an image current in the structure due to the current flowing through the conductor of the inductive element 14.

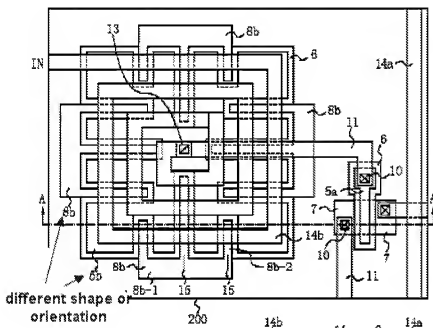
With respect to amended claims 1 and 3 the limitation, *"wherein the arrangement of the tilling structures is determined by a desired pattern density of the semiconductor device for improving at least one of a process window of lithography, uniformity of Chemical Mechanical Polishing removal rate and integrity of low-k dielectrics"*, this has been considered but not given any patentable weight. "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ964, 966 (Fed. Cir. 1985).

Hiromoto has the desired pattern density in its tilling structure, as shown in Figure 1.



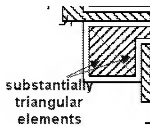
With regards to claim 4, Applicant argues that the cited portions 5b and 8b of Hiromoto are have the same shape and orientation. The Examiner disagrees.

Shown in this annotated Figure of Hiromoto (Figure 1) that 5b and 8b are of different shape and orientation.



With regards to claim 8, Applicant argues that Hiromoto reference does not correspond to aspects of the claimed invention directed to the tiling structures being a plurality of substantially triangular elements. That is not correct.

The tiling structure of Hiromoto as shown in Figure 1 or 3 shows each four corners(5b) having a shape corresponding to two substantially triangular shape elements (close to being a triangle) having a common side forming a substantially square shape. Annotated portion of Hiromoto's Figure 3 is shown below.



With regards to claims 14, 15 and 16, Applicant argues that Hiromoto discuss parasitic capacitance and not a separate passive element.

It would have been obvious to one having ordinary skill in the art at the time of the invention to produce a passive element, i.e., capacitor, (if needed in the circuit) since the structure of Hiromoto discloses capacitive properties being present in its structure.

### *Conclusion*

The applicant's amendment has been fully considered. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however,

will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joselito Baisa whose telephone number is (571) 272-7132. The examiner can normally be reached on M-F 5:30 am to 2:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Elvin Enad can be reached on (571) 272-1990. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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